CMP\_BIST\_CTRL

Revision History

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| --- | --- | --- | --- |
| Revision Number | Date | Description of Change | Author |
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# CMP\_BIST\_CTRL

## Introduction

CMP\_BIST\_CTRL is mainly used for functional safety to check whether VAA\_OVUV, VDD\_OVUV\_BIST, CP\_OVUV, AGND\_OW fault can be generated correctly.

### Main features

The CMP\_BIST\_CTRL module has the following features:

•Supports output 400us BIST\_REF\_EN high pulse and 200us BIST\_REF\_EN\_EARLY high pulse when BIST\_GO is detected (HWSR2\_CMP\_BIST\_CTRL)

•CMP\_BIST\_CTRL shall be reset when CLK\_32M\_OK is low (HWSR1\_CMP\_BIST\_CTRL)

Supports output clr\_BIST\_GO after BIST\_GO is detected (HWSR3\_CMP\_BIST\_CTRL)

• Before BIST\_REF\_EN\_EARLY turns low, CMP\_BIST\_CTRL shall check if VAA\_OVUV, VDD\_OVUV\_BIST, CP\_OVUV, AGND\_OW are all 1 within 50us, if any is 0, output CMP\_FLT (HWSR4\_CMP\_BIST\_CTRL)

## Functional Details

### Block Diagram



Fig 1 CMP\_BIST\_CTRL Block Diagram

### I/O description

Table 1 CMP\_BIST\_CTRL I/O description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Name** | **Direction** | **Duration** | **Width** | **Description** |
| **BIST\_GO** | I | N/A | 1b’ | To start CMP\_BIST\_CTRL |
| **VAA\_OV** | I | N/A | 1b’ | VAA\_OV fault |
| **VAA\_UV** | I | N/A | 1b’ | VAA\_UV fault |
| **CP\_OV** | I | N/A | 1b’ | CP\_OV fault |
| **CP\_UV** | I | N/A | 1b’ | CP\_UV fault |
| **AGND\_OW** | I | N/A | 1b’ | AGND\_OW fault |
| **VDD\_OV\_BIST** | I | N/A | 1b’ | VDD\_OV\_BIST fault |
| **VDD\_UV\_BIST** | I | N/A | 1b’ | VDD\_UV\_BIST fault |
| **CLK\_32M\_OK** | I | N/A | 1b’ | CMP\_BIST\_CTRL shall be reset when CLK\_32M\_OK is low |
| **CLK\_REG\_SC** | I | N/A | 1b’ | Clock for CMP\_BIST\_CTRL |
| **resetb\_SR\_CLK\_REG** | I | N/A | 1b’ | Reset signal |
| **clr\_BIST\_GO** | O | 1 CLK\_REG\_SC | 1b’ | To clear BIST\_GO |
| **CMP\_FLT** | O | 1 CLK\_REG\_SC | 1b’ | Detect CMP\_BIST fault |
| **BIST\_REF\_EN** | O | 400 us | 1b’ | Output 400us BIST\_REF\_EN high pulse |
| **BIST\_REF\_EN\_EARLY** | O | 200us | 1b’ | Output 200us BIST\_REF\_EN\_EARLY high pulse |

### Fault detect

(HWSR1\_CMP\_BIST\_CTRL, HWSR2\_CMP\_BIST\_CTRL, HWSR3\_CMP\_BIST\_CTRL, HWSR4\_CMP\_BIST\_CTRL)

Fig 2 Waveform diagram of CMP\_BIST\_CTRL

When CB\_GO arrives, CMP\_BIST\_CTRL outputs 400ns BIST\_REF\_EN and 200ns BIST\_REF\_EN\_EARLY. At the two CLK\_REG\_SC cycles before BIST\_REF\_EN\_EARLY disappears, CMP\_BIST\_CTRL will detect all faults. If any FAULT is 0, CMP\_FALUT will be generated, indicating that FALULT cannot be generated correctly for the module.